



Leakage in Nanometer CMOS Technologies (Integrated Circuits and Systems)

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Covers in detail promising solutions at the device, circuit, and architecture levels of abstraction after first explaining the sensitivity of the various MOS leakage sources to these conditions from the first principles.

Also treated are the resulting effects so the reader understands the effectiveness of leakage power reduction solutions under these different conditions.

Case studies supply real-world examples that reap the benefits of leakage power reduction solutions as the book highlights different device design choices that exist to mitigate increases in the leakage components as technology scales.

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